Design and Evaluation of High Performance Multiplier Using Modified Booth Encoding Algorithm

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Abstract: - In this paper multipliers are used for high performance embedded cores and in all multiplier designs. In conventional two's complement multiplier the main problem is that it requires more computation time. In this paper Computation time of the Two's complement multiplier is reduced by decreasing the maximum height of the partial product array by one row in a radix-4 Modified Booth Encoded Multiplier. The classic two's complement nxn bit multiplier using the radix 4 MBE scheme generates a partial product(PP) array with a maximum height of n/2+1 rows, here we are going to reduce the maximum height of PP array to n/2. This technique allows for faster compression of the partial product array without any increase in the delay and can be extended to higher radix encodings. This technique mostly relies on circuit optimization and minimization of the critical paths. We are using Cadence RTL compiler for synthesize report and Model simulator for simulation results.

Keywords: **Multiplication Modified Booth Encoding, Partial Product Array.**

1. INTRODUCTION

In multimedia, 3D graphics and signal processing applications, performance, in most cases[1], strongly depends on the effectiveness of the hardware used for computing multiplications, since multiplication is, besides addition, massively used in these environments[2][10]. The high interest in this application field is witnessed by the large amount of algorithms and implementations of the multiplication operation, which have been proposed in the literature (for a representative set of references, see [6],[9]). More specifically, short bit-width (8-16 bits) two's complement multipliers with single-cycle throughput and latency have emerged and become very important building blocks for high-performance embedded processors and DSP execution cores [7], [5]. In this case, the multiplier must be highly optimized to fit within the required cycle time and power budgets. Another relevant application for short bit-width multipliers is the design of SIMD units supporting different data formats [6], [7]. In this case, short bit-width multipliers often play the role of basic building blocks.

II. MODIFIED BOOTH ENCODING (MBE) TECHNIQUE

The basic algorithm for multiplication is based on the well-known paper and pencil approach [5],[6] and passes through three main phases: 1) partial product (PP) generation, 2) PP reduction, and 3) final (carry-propagated) addition[7],[12]. Booth recoding can be extended for a redundant multiplier operand [4]. While [4] starts with a signed-bit Booth recoder and adds a special pre processing step in order to deal with a carry-save operand, the redundant Booth recoder in this work base been optimized for the carry-save representation and reduces the critical path by one XOR gate. During PP generation, a set of rows is generated where each one is the result of the product of one bit of the multiplier by the multiplicand. For example, if we consider the multiplication $X \times Y$ with both X and Y on n bits and of the form $xn\_1 \ldots x0$ and $yn\_1 \ldots y0$, then the ith row is, in general, a proper left shifting of $yi \times X$, i.e., either a string of all zeros when $yi = 0$, or the multiplicand X itself when $yi = 1$. In this case, the number of PP rows generated during the first phase is clearly n. Modified Booth Encoding (MBE) [3] is a technique that has been introduced to reduce the number of PP rows, still keeping the generation process of each row both simple and fast enough[7],[9]. One of the most commonly used schemes is radix-4 MBE, for a number of reasons, the most important being that it allows for the reduction of the size of the partial product array by almost half[3], and it is very simple to generate the multiples of the multiplicand. More specifically, the classic two's complement n × n bit multiplier using the radix- 4 MBE scheme, generates a PP array with a maximum height of [n/2]+1 rows[4], each row before the last one being one of the following possible values: all zeros, $\pm X; \pm 2X$. The last row, which is due to the negative encoding, can be kept very simple by using specific techniques integrating two's complement and sign extension prevention [6],[10]. In this work, we introduce an idea to overlap, to some extent, the PP generation and the PP reduction phases. Our aim is to produce a PP array with a maximum height of [n/2] rows that is then reduced by the compressor tree stage.
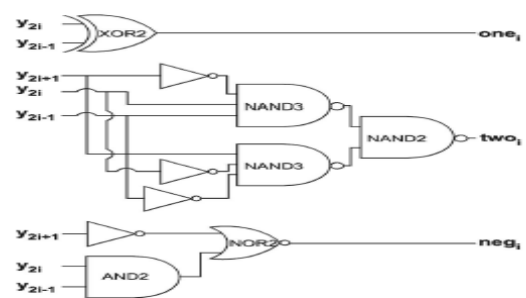
III. DESIGN FLOW

Fig 1: MBE Signal Generation

A. *Explanation of design flow:*

Let us take two 8-bit input vectors, A & B are two 8-bit vector inputs and P is the output vector.

A = 0 0 0 1 0 0 1 1   (1 9) applying

MBE RULES:

> ➢ Pad LSB with 1 zero
>
>   0 0 0 1 0 0 1 1 0
>
> ➢ n is even then pad the MSB with two zeros
>
>   0 0 0 0 0 1 0 0 1 1 0
>
> ➢ Form 3-bit overlapping groups for n=8 we have 5 groups

A[10]A[9] A[8]A[7]A[6]A[5]A[4]A[3] A[2] A[1] A[0]

  0   0   0   0   0   1   0   0   1   1   0

From right to left each bit will be assigned in the below way

1) .y2i-1=0   2). Y2i-1=1   3). Y2i-1=0

   Y 2i=1   Y 2i=0   Y 2i=1

   Y 2i+1=1   Y 2i+1=0   Y 2i+1=0

4) .y2i-1=0   5). Y2i-1=0

   Y 2i=0   Y 2i=0

Table1: Partial product outputs:

PP[8]	PP[7]	PP[6]	PP[5]	PP[4]	PP[3]	PP[2]	PP[1]	PP[0]
pp0[8:0] = 0	1	1	1	1	1	0	1	0
pp1[8:0]= 1	0	0	0	0	0	1	0	1
pp2[8:0]= 1	0	0	0	0	0	1	0	1
pp3[8:0]= 0	0	0	0	0	0	0	0	0

  Y 2i+1=0   Y 2i+1=0

Assign to all bits in MBE Signal Generation circuit then MBE out puts are below

1) Onei1 = 1   3) onei3 = 1

   Twoi1 = 0   Twoi3 = 0

   Negi1 = 0   Negi3 = 0

2) Onei2 = 1   4) onei4 = 1

   Twoi2 = 0   Twoi4 = 0

   Negi2 = 0   Neg14 = 0

Similarly applying 8-bit B vector to Partial Product Generation circuit

B= 0   0   0   0   1   0   1   1   (11)

Applying MBE rules then

B[9] B[8] B[7] B[6] B[5] B[4] B[3] B[2]B[1]B[0]

  0   0   0   0   0   1   0   1   1   0

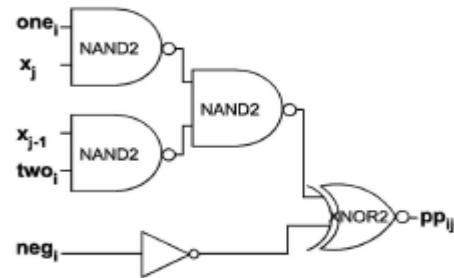> ➢ Form 2-bit overlapping groups for n=8 we have 9 groups.

FIG 2: Partial Product Generation

1)Xj-1=0   2) Xj-1=1   3)Xj-1=1

   Xj =1   Xj =1   Xj =0

4)Xj-1=0   5)Xj-1=1   6)Xj-1=0

   Xj =1   Xj =0   Xj =0

7)Xj-1=0   8)Xj-1=0

   Xj =0   Xj =0

Assign to all bits in Partial Product Generation circuit then Partial Product Generation out puts are below

  PP [0 0] =0, PP [01] =0 PP [02] =1…………....…PP [09] =1

A.A. *(A and B) Multiplication:*

              A 0 0 0 1 0 0 1 1
              B 0 0 0 0 1 0 1 1

          1 1 1 1 1 0 1 0 0

        0 0 0 0 0 1 0 1 1 0 1……… negi1

       0 0 0 0 0 1 0 1 1 0 0 0 0………. negi2

      0 0 0 0 0 0 0 0 0 0 0 0 0 0………….... negi3

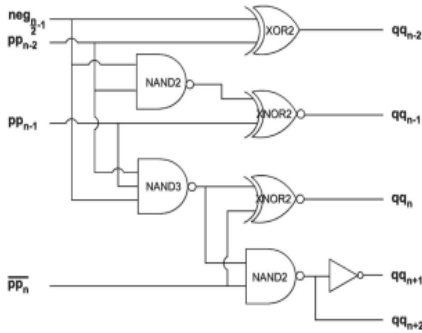 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0…………………….negi4

Fig 3: Gate-Level Diagram Of Proposed Of the Method Is For Adding The Last Neg Bit In The First Row

The above figure shows the gate level diagram of proposed of the method is for adding the last neg bit in the first row i.s last negative bit is added to first row($0 \rightarrow 1$ or $1 \rightarrow 0$).

A=0 0 0 1 0 0 1 1 (19)

B= 0 0 0 0 1 0 1 1 (11)

0 0 0 0 0 0 1 1 1 1 1 1 0 1 0 0 – in1

0 0 0 0 1 0 0 0 0 0 1 0 1 1 0 1 – in2

0 0 1 0 0 0 0 0 1 0 1 1 0 0 0 0 – in3

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 – in4

0 0 0 0 0 0 0 0 1 1 0 1 0 0 0 1 $\rightarrow$ (209)

IV. RESULTS

A. Synthesize report:

Fig: 4 shows the Booth multiplication top view diagram and Fig: 5 Booth multiplications RTL internal diagram using Xilinx 12.0 version. Fig: 7 synthesize report of Booth multiplication using Cadence RTL compiler
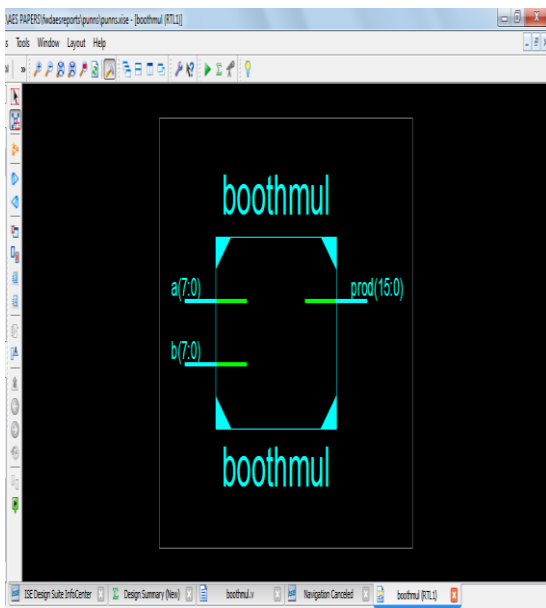

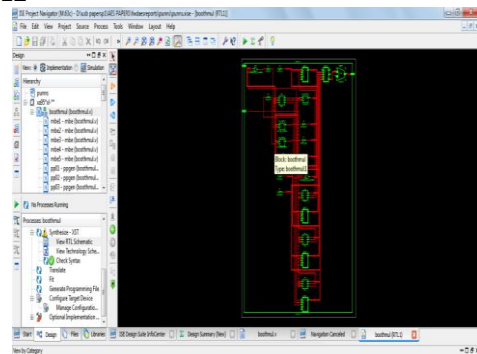**Fig: 4 Booth multiplication top view (RTL) diagram**

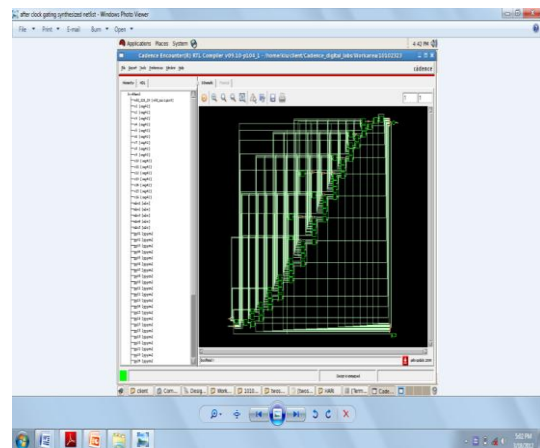**Fig: 5 Booth multiplication RTL internal diagram**

Fig: 6 synthesize report of Booth multiplication using Cadence RTL compiler

B.Power report

```
=====================================
=========
  Generated by: Encounter(R) RTL
Compiler
  Generated on:        Feb 27 2012
04:44:15 PM
  Module:              boothmul
  Technology library:  tsmc18 1.0
  Operating conditions:  slow
(balanced_tree)
  Wireload mode:       enclosed
  Area mode:           timing
library
=====================================
=========

              Leakage   Dynamic
Total
Instance Cells Power (nW) Power (nW)
Power (nW)
--------------------------------------
---------
boothmul   139 158.764 322502.747
322661.510
```

C. Simulation Results

Fig 7:Shows the Simulation results of Booth Multiplication using ModelSim Simulator input bits are A=00001011,B=00010011 then output is 0000000010 .
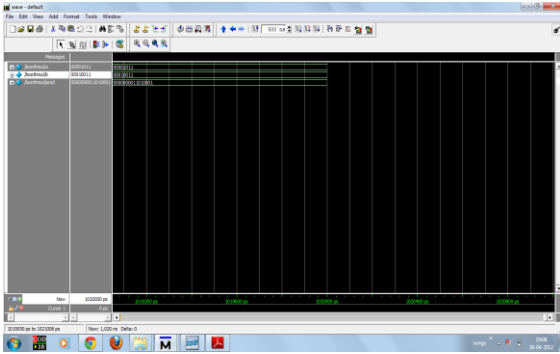
Fig 7: Simulation results of Booth Multiplication using Modelsim Simulator

V. CONCLUSION

With the extra hardware the maximum height of the partial product array has been reduced by one unit. No extra delay in the Partial product generation stage with reduction of maximum height.

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